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FOR

REFRESH METHODS FOR RAM CELLS FEATURING HIGH SPEED ACCESS

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DESCRIPTION OF THE INVENTION

Field of the Invention

[001] This invention pertains in general to a memory device and more particularly, to a system and method for operating a memory device.

Background of the Invention

[002] Random access memory ("RAM") devices are typically used as storage devices in various applications such as computer systems, mobile phones, and video systems. A RAM device may include a dynamic RAM ("DRAM") and a static RAM ("SRAM"). A DRAM cell generally includes a capacitor and a transistor, and therefore is advantageously small in area. Data are stored in the capacitor of a DRAM cell in the form of electric charges. The charges stored in the capacitor might be lost over time and therefore need to be restored periodically by refresh operations. A refresh operation is a process of recharging the cells in a memory chip. Cells are refreshed, for example, one row per refresh cycle.

[003] An SRAM cell generally includes a flip-flop circuit. As compared to a DRAM cell, an SRAM cell has fast access time with no refresh operation required. However, an SRAM cell, which may include six transistors, is relatively large in size and consumes more power than a DRAM cell per bit.

[004] A pseudo-SRAM cell is known in the art for its combined advantages of a DRAM and SRAM cells. Although a capacitor is used to store data in a cell, a refresh operation is "hidden" or "concealed" in the pseudo-SRAM cell. Examples of pseudo-SRAM cells include U.S. Patent No. 4,549,284 to Ikuzaki, entitled "Dynamic

MOS Random Access Memory," No. 6,028,804 to Leung, entitled "Method and Apparatus for 1-T SRAM Compatible Memory," and No. 6,625,077 to Chen, entitled "Asynchronous Hidden Refresh of Semiconductor Memory."

[005] There is a general need in the art to have a pseudo-SRAM cell to include the advantages of scheduled refresh and access cycles and reduced access cycle time.

SUMMARY OF THE INVENTION

[006] Accordingly, the present invention is directed to a system and a method that obviate one or more of the problems due to limitations and disadvantages of the related art.

[007] To achieve these and other advantages, and in accordance with the purpose of the invention as embodied and broadly described, there is provided a memory system that comprises a memory device further comprising an array of cells formed in rows and columns, a control signal controlling operation modes of the memory device, and a generator receiving the control signal providing a refresh request at a same period if the control signal is deactivated, providing no refresh request in response to a first state of the control signal if the control signal is activated, and providing a refresh request in response to a second state of the control signal if the control signal is activated.

[008] Also in accordance with the present invention, there is provided a method of operating a memory device including an array of cells formed in rows and columns that comprises providing a control signal, activating the control signal, the activated control signal including a first state and a second state, continuously

performing access cycles in response to the first state of the activated control signal in one part of a period, and continuously performing refresh cycles in response to the second state of the activated control signal in another part of the period.

[009] Further in accordance with the present invention, there is provided a method of operating a memory device including an array of cells formed in rows and columns that comprises providing a control signal including a first state and a second state, determining a period within which each of the cells is refreshed before data stored therein are lost, determining the number of refresh cycles to perform in the period, performing at least one refresh cycle in response to the second state of the control signal, and allowing at least one access cycle to perform in response to the first state of the control signal.

[010] Still in accordance with the present invention, there is provided a method of operating a memory device including an array of cells formed in rows and columns that comprises providing a control signal, deactivating the control signal by connecting the control signal to a fixed level, providing a refresh request at a same period, activating the control signal, providing no refresh request in response to a first state of the activated control signal, and providing at least one refresh request in response to a second state of the activated control signal.

[011] Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[012] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

[013] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate one embodiment of the invention and together with the description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[014] Fig. 1A is a block diagram of a memory system in accordance with one embodiment of the present invention;

[015] Fig. 1B is a diagram of an array of memory cells shown in Fig. 1A;

[016] Fig. 1C is a diagram of a refresh generator shown in Fig. 1A;

[017] Figs. 1D, 1E and 1F are timing diagrams of a control signal and a refresh clock in accordance with one embodiment of the present invention;

[018] Fig. 2A is a diagram showing an access operation in accordance with one embodiment of the present invention;

[019] Fig. 2B is a diagram showing a refresh operation in accordance with one embodiment of the present invention;

[020] Fig. 3A is a diagram showing an access operation in accordance with another embodiment of the present invention;

[021] Fig. 3B a diagram showing an access operation in accordance with still another embodiment of the present invention;

[022] Fig. 4 is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention;

[023] Fig. 5A is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention;

[024] Fig. 5B is a diagram showing a method of operating a memory device in accordance with another embodiment of the present invention;

[025] Fig. 5C is a diagram showing a method of operating a memory device in accordance with still another embodiment of the present invention;

[026] Fig. 6 is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention; and

[027] Fig. 7 is a diagram showing a method of operating a memory device in accordance with yet another embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[028] Reference will now be made in detail to the present embodiment of the invention, an example of which is illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[029] Fig. 1A is a block diagram of a memory system 10 in accordance with one embodiment of the present invention. Memory system 10 includes an array of memory cells 201, a row decoder 202, an amplifier unit 203, a column decoder 204, an address buffer 206, and a refresh generator 207. Memory system 10 further includes a control signal REFEN used to control operation modes of memory system 10, which will be discussed below. In one embodiment according to the invention, control signal REFEN is externally controllable by a user. Memory cells 201,

amplifier unit 203 and column decoder 204 are further illustrated in Fig. 1B. Refresh generator 207 is further illustrated in Fig. 1C.

[030] Referring to Fig. 1B, memory cells 201 are formed in rows and columns in a matrix. For discussion, only rows 291, 292 and 293, and columns 281, 282, 283 and 284 are numbered. Amplifier unit 203 includes a plurality of sense amplifiers 231, 232, 233, 234, ...corresponding to column lines 281, 282, 283, 284, ... respectively. Each of the sense amplifiers senses a signal level on a corresponding column line and amplifies the signal level. Column decoder 204 includes a plurality of pass gates 241, 242, 243, 244, ...corresponding to sense amplifiers 231, 232, 233, 234, ..., respectively. Column decoder 204 is connected to a data input/output buffer 205 through which data are read out or written in.

[031] Referring to Fig. 1C, refresh generator 207 further includes an oscillator 301, a refresh controller 302, and a refresh address generator 303. Oscillator 301 receives control signal REFEN, and provides a refresh clock REFCLK to refresh controller 302 and refresh address generator 303. In one embodiment according to the invention, control signal REFEN is deactivated, for example, by being connected to a fixed voltage level. In response to a deactivated control signal REFEN, oscillator 301 provides refresh clock REFCLK at a plurality of sub-periods tRP within a period tREFmax. The period tREFmax refers to a maximum time interval within which each particular cell 201 should be refreshed before data stored therein are lost. A sub-period tRP refers to one within which a refresh operation or a refresh cycle should be performed. Each of sub-periods tRP is equal to tREFmax divided by N, where N is the number of total refresh cycles performed for the array of

cells 201 within the interval tREFmax. Oscillator 301 may include a timer (not shown) for periodically generating refresh clock REFCLK at sub-periods tRP. In one embodiment according to the invention, a total number of 4096 refresh cycles are performed within 64 ms (milliseconds). For an 8Mb memory device having 512K rows, a refresh operation is performed approximately every 10 μs (microseconds) to 15 μs.

[032] In another embodiment according to the invention, control signal REFEN is activated, which includes a first state and a second state. The first state may include a logic low state, and the second state may include a logic high state. In response to the first state of an activated control signal REFEN, oscillator 301 and refresh generator 207 are turned off. In response to the second state of an activated control signal REFEN, oscillator 301 is turned on and provides a refresh clock REFCLK at a plurality of sub-periods tRP1, tRP2 ... and tRPN within tREFmax. Each of sub-periods tRP1, tRP2 ... and tRPN may be different from tRP.

[033] Figs. 1D, 1E and 1F are timing diagrams of control signal REFEN and refresh clock REFCLK. Referring to Fig. 1D, when control signal REFEN is deactivated, refresh clock REFCLK is generated periodically every tRP. Referring to Fig. 1E, when control signal REFEN is activated, refresh clock REFCLK is generated in response to a high logic state of control signal REFEN. Referring to Fig. 1F, refresh clock REFCLK rises and falls with control signal REFEN if a pulse width PW of control signal REFEN is smaller than half a tRP, which allows more than one refresh clock REFCLK to be provided and in turn more than one refresh cycle to perform within tRP.

[034] Referring again to Fig. 1A, address buffer 206 receives an input address signal AIN during an access operation, and provides a latched address signal LADD to a multiplexer 208 when input address signal AIN is latched. Address buffer 206 also provides an access request ACCREQ to a signal controller 209 for an access operation for a row of cells 201 corresponding to latched address signal LADD. Refresh generator 207 receives control signal REFEN, and provides a refresh address signal REFADD to multiplexer 208 and a refresh request REFREQ to signal controller 209 for a refresh operation for a row of cells 201 corresponding to refresh address signal REFADD. Signal controller 209 may include an arbiter circuit (not shown) to determine the priority of access request ACCREQ and refresh request REFREQ, and provides a selection signal SEL to multiplexer 208. Signal controller 209 also provides a column address AY to column decoder 204. Meanwhile, in response to signals LADD, REFADD and SEL, multiplexer 208 provides a row address AX to row decoder 202. An access or a refresh operation, depending on selection signal SEL, is then performed for one of cells 201 corresponding to the row address AX and column address AY.

[035] Fig. 2A is a diagram showing an access operation in accordance with one embodiment of the present invention. When control signal REFEN is deactivated, access cycles are allowed to perform until a refresh request is made. Referring to Fig. 2A, an access request ACCREQ is pulled high whenever an access address signal AIN is asserted. Row decoder 202 and column decoder 204 respectively selects a corresponding row and column of a memory array. In the particular embodiment shown in Fig. 2A, only read cycles are illustrated. However,

skilled persons in the art will understand that an access cycle may include one of a read cycle or a write cycle. A read cycle, performed for an access time of tAA0, includes a first period R and a second period P. The first period R covers the time for selecting a corresponding row and sensing data stored in the row of cells. The second period P covers the time for switching pass gates and sending selected data for output. For an 8Mb memory device with a bandwidth of 16, the read access time tAA0 is approximately 20 ns (nanoseconds) to 80 ns.

[036] Fig. 2B is a diagram showing a refresh operation in accordance with one embodiment of the present invention. When control signal REFEN is deactivated and a refresh cycle occurs in response to a refresh clock REFCLK periodically generated at tRP, a refresh operation is performed. The refresh operation is "hidden" from a user because it is automatically performed. Since a periodic refresh operation may occur before or after a pending access operation, a refresh request REFREQ regarding the refresh operation and an access request ACCREQ regarding the access operation are compared to each other in signal controller 209 to determine which operation to perform first. A resultant access time including a refresh operation, performed for a time of tAA1 greater than tAA0, includes a third period F in addition to the first period R and the second period P. The third period F covers the time for selecting a corresponding row and restoring data in the row, and has a same time length as the first period R. Time tAA1 is measured from a time an address access signal AIN is asserted to a time selected data are output. Therefore, the length of tAA1 is directly dependent on the time

access address signal AIN is asserted. That is, the earlier AIN is asserted, the greater length tAA1 has.

[037] Fig. 3A is a diagram showing an access operation in accordance with another embodiment of the present invention. Control signal REFEN, when activated, includes a first state and a second state. In response to the first state of an activated control signal REFEN, oscillator 301 is turned off and therefore no refresh request is made. Access cycles are allowed to perform until a refresh request is made. Referring to Fig. 3A, access cycles are continuously performed without being interrupted or compromised by periodic refresh cycles, resulting in a reduction of total access time. Each of the access cycles includes a first period R and a second period P and is performed for an access time of tAA0.

[038] Fig. 3B is a diagram showing an access operation in accordance with still another embodiment of the present invention. Control signal REFEN is activated and held at the first state. A plurality of access cycles are continuously performed without interruption of refresh cycles. In a first period R of a first access cycle, a row address signal AX is asserted to select a row of cells 201, and data stored in the row of cells 201 are sensed by the sense amplifiers. In a second period P of the first access cycle following the first period R, a column address signal AY is asserted to switch pass gates, and selected data are sent for output. The access time for the first access cycle is tAA0. For the remaining access cycles, the same row of cells 201 is kept for data access. As a result, only the second period P is spent for each of the remaining access cycles. The access time for each of the remaining cycles is

tP. Since no new row is selected in the access cycles, a time-consuming row changing is eliminated, resulting in a further reduction of total access time.

[039] Fig. 4 is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention. The method uses a control signal REFEN to control operation modes of a memory device. When control signal REFEN is activated, the memory device is operated in a first mode or access mode in response to a first state of the activated control signal REFEN. In the first mode, access cycles are continuously performed without interruption of refresh cycles, which has been discussed in conjunction with Figs 3A and 3B. The memory device is operated in a second mode or refresh mode in response to a second state of the activated control signal, which will be discussed in conjunction with Figs. 5A to 5C. An activated control signal REFEN has a pulse width PW smaller than half a tRP, and therefore allows continuous access cycles or continuous refresh cycles to perform. When control signal is deactivated, for example, by being connected to a fixed voltage level, the memory device is operated in a mode in which a refresh cycle is periodically generated at each of sub-periods tRP, which has been discussed in conjunction with Figs. 2A and 2B.

[040] Fig. 5A is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention. Refresh cycles are continuously performed in one part of tREFmax in a refresh mode without interruption of access cycles, and access cycles are continuously performed in the other part of tREFmax.

[041] Fig. 5B is a diagram showing a method of operating a memory device in accordance with another embodiment of the present invention. A refresh cycle is performed when tREFmax or one of sub-periods tRP occurs. Access cycles are allowed to perform between two consecutive refresh cycles until tREFmax or tRP occurs.

[042] Fig. 5C is a diagram showing a method of operating a memory device in accordance with still another embodiment of the present invention. Refresh cycles are performed at sub-periods tRP1, tRP2 ... tRPN within tREFmax. Each of sub-periods tRP1, tRP2 ... tRPN may be different from tRP.

[043] Fig. 6 is a diagram showing a method of operating a memory device in accordance with one embodiment of the present invention. By changing the number of total refresh cycles N, the refresh period is changed. In the upper part of Fig. 6, a refresh cycle of N refresh cycles is performed at every tRP. In the lower part of Fig. 6, a refresh cycle of N/2 refresh cycles is performed at every tRP', two times tRP.

[044] Fig. 7 is a diagram showing a method of operating a memory device in accordance with yet another embodiment of the present invention. By maintaining control signal REFEN at the second state, an "auto-refresh" is performed within tREFmax for the entire array of cells by refreshing all rows in turn.

[045] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.